SEMICONDUCTOR DEVICE AND
METHOD OF MANUFACTURING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

5   This application is based upon and claims the benefit of priority from prior Japanese Patent Applications No. 2002-282441, filed on September 27, 2002 and No. 2003-320316, filed on September 11, 2003, the entire contents of which are incorporated herein by reference.

10   ## BACKGROUND OF THE INVENTION
Field of the Invention

          The present invention relates to a semiconductor device and a method of manufacturing the same. In particular, the present invention relates to a MOS (metal-oxide-semiconductor)
15   semiconductor device, in which the reliability of thin dielectric films, such as gate oxide layers, is increased, and a method of manufacturing the same.
Related Art

          Recently, as the performance and speed of LSIs (large scaled
20   integrated circuits) are improved, the miniaturization of MOS transistors has advanced. Accordingly, there have also been rapid advances in decreasing the thickness of gate dielectric films of MOS transistors. As a result, there is a demand for a technique for uniformly forming an ultra-thin silicon dielectric film
25   uniformly with a high reliability. It was recently reported that a device first suffering soft breakdown (SBD) and then reaching hard breakdown (HBD), as a dielectric breakdown mode, has a longer lifetime than a device first suffering hard breakdown (K. Okada et al., Tech Dig. Symp. on VLST Technology, p. 57 (2000); K. Okada
30   et al., "A Concept of Gate Oxide Lifetime Limited by "B-mode" Stress Induced Leakage Currents in Direct Tunneling Regime", Symposium on VLSI Technology Digest of Technical Paper, 1999, PP. 57 - 58). However, since whether a dielectric breakdown of a gate dielectric film is a soft breakdown or a hard breakdown
35   is dependent on random chance, it has been very difficult to selectively cause only soft breakdown. A device suffering soft

breakdown has a significantly longer lifetime (a period from the time a device suffers soft breakdown to the time it reaches hard breakdown) when it is used under a low voltage stress than when it is used under a high voltage stress. This is shown in Fig.

5   8, in which the horizontal axis represents stress voltage (-V) applied to the gate of a device, and the vertical axis represents lifetime (S). That is, T_{HB} shows the period (lifetime) from the time a device suffers soft breakdown to the time it reaches hard breakdown. As can be understood from Fig. 8, the gradient of

10   the graph changes when the stress voltage is less than about 3.2 V. This means that when the stress voltage is under about 3.2 V, the lifetime is extended.

As described above, a dielectric breakdown of a gate dielectric film is believed that once a soft breakdown occurs

15   then a hard breakdown occurs. However, in general, there has been a problem in that technically it is not possible to control the time from the point a soft breakdown occurs to the point a hard breakdown occurs.

20   SUMMARY OF THE INVENTION

The present invention is proposed in consideration of the above-described circumstances. The characteristic feature of the present invention lies in that although defective portions are caused by non-uniform implantation of an impurity to a gate

25   dielectric film, which implantation forming portions electrically weak against stress, it is possible to maintain the dielectric breakdown mode of the gate dielectric film at the soft breakdown level. It is the object of the present invention to provide a semiconductor device having a structure capable of lengthening

30   the hard breakdown lifetime of its gate dielectric film, this semiconductor device being easy to manufacture at a low cost, and having a high reliability, and a method of manufacturing such a semiconductor device.

The embodiment of the present invention is directed to a

35   semiconductor device including: a semiconductor substrate of a first conductivity type; a channel region formed at a surface

of the semiconductor substrate; source and drain regions of a second conductivity type formed at both sides of the channel region in the semiconductor substrate; an insulating layer covering the channel region; and a gate electrode formed on the insulating layer, the insulating layer containing impurity atoms in such a manner that a concentration thereof is non-uniformly distributed along a surface parallel to the semiconductor substrate.

The embodiment of the present invention is further directed to a method of manufacturing a semiconductor device including: forming an insulating layer on a semiconductor substrate of a first conductivity type; forming a conductive layer on the insulating layer; forming on the conductive layer a spotted layer including minute spots containing a resistive material resisting against ion implantation; non-uniformly implanting impurity ions to the conductive layer via the spotted layer containing the resistive material; and diffusing the impurity ions in the conductive layer into the insulating layer.

The embodiment of the present invention is still further directed to a method of manufacturing a semiconductor substrate comprising: forming an insulating layer on a semiconductor substrate of a first conductivity type; forming a conductive layer on the insulating layer; performing implantation of impurity ions several times so that an impurity concentration of the conductive layer becomes non-uniform due to implantation fluctuations; and diffusing the impurity ions in the conductive layer into the insulating layer.

The embodiment of the present invention is further directed to a method of manufacturing a semiconductor substrate comprising: forming an insulating layer on a semiconductor substrate of a first conductivity type; forming a conductive layer on the insulating layer; forming minute projections and depression on a surface of the conductive layer by etching the conductive layer; performing ion implantation of impurity ions on the conductive layer having the projections and depressions on the surface; and diffusing the impurity ions in the conductive layer into the insulating layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a sectional view showing the structure of a MOS type transistor according to the first embodiment of the present invention.

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Figs. 2(a) to 2(f) are sectional views showing the steps of a method of manufacturing a MOS type transistor according to the second embodiment of the present invention.

Figs. 3(a) to 3(f) are sectional views showing the steps of a method of manufacturing a MOS type transistor according to the third embodiment of the present invention.

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Figs. 4(a) to 4(f) are sectional views showing the steps of a method of manufacturing a MOS type transistor according to the fourth embodiment of the present invention.

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Fig. 5 shows the cumulative fraction defective of the total amount (Qbd) of electrons passing through the gate oxide layer before a dielectric breakdown occurs, with the dose amount of fluorine being changed.

Fig. 6 shows the lifetime distribution of MOS capacitors manufactured according to the present invention.

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Fig. 7 shows the frequency of occurrence of initial soft breakdown of MOS capacitors manufactured according to the present invention.

Fig. 8 shows that the hard breakdown lifetime of a MOS structure is lengthened if it first suffers a soft breakdown.

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Fig. 9 shows the relationship between the highest fluorine concentration in layer divided by the lowest fluorine concentration in layer and the frequency initial occurrence of soft breakdown.

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DESCRIPTION OF THE EMBODIMENTS

Hereinafter, the embodiments of the present invention will be described with reference to the accompanying drawings.

35   (First Embodiment)

Fig. 1 shows a cross-sectional structure of a MOS type semiconductor device according to the first embodiment of the present invention. The MOS type semiconductor device of this embodiment includes, for example, an n-type silicon substrate 1 having a surface orientation (100), and a specific resistance of 4 - 6 Ωcm, and device isolation regions 2a and 2b, which are about 0.6 μm in depth, formed in the silicon substrate 1. A gate oxide layer 4a having a thickness of, e.g., 2 - 8 nm, is formed on the silicon substrate 1 by thermal oxidation, and a polycrystalline silicon layer 5a serving as a gate electrode is formed on the gate oxide layer 4a, the polycrystalline silicon layer 5a having a thickness of 200 nm. The gate electrode contains, e.g., $3 - 5 \times 10^{20}$ cm^{-3} of phosphorous serving as a dopant to decrease the resistance of the gate electrode. The gate insulating layer 4a contains, e.g., $1 \times 10^{19} - 1 \times 10^{20}$ cm^{-3} of fluorine atoms serving as impurities, the fluorine atoms being distributed in the gate insulating layer such that the highest fluorine concentration is more than two times as large as the lowest fluorine concentration in a parallel cross section to the surface of silicon substrate. The present inventor has understood from his experience that as shown in Fig. 9, when the highest fluorine concentration is more than two times as large as the lowest, the dielectric breakdown of the gate dielectric film is maintained to be within the range of soft breakdown. Impurity layers 10 serving as a pair of source and drain diffusion layers are located at both sides of the gate electrode in the silicon substrate 1, on each of which a titanium silicide layer 13 is formed. A gate sidewall 11 of silicon nitride is formed around the gate electrode. A silicon oxide layer 14 is deposited on the entire device, through which contact holes 15 are formed. Aluminum electrodes 16 connecting to the gate electrode and the source and drain diffusion layers are formed via the contact holes 15.

As described above, according to the this embodiment, the gate oxide layer contains, e.g., $1 \times 10^{19} - 1 \times 10^{20}$ cm^{-3} of fluorine atoms serving as impurities, the fluorine atoms being distributed in the gate oxide layer such that the highest fluorine concentration

is more than two times as large as the lowest fluorine concentration in a parallel cross section to the surface of silicon substrate 1. This enables the dielectric breakdown of the gate dielectric film to be maintained in the soft breakdown mode, and also enables the lengthening of the hard breakdown lifetime of the gate dielectric film.

Although $1 \times 10^{19} - 1 \times 10^{20}$ cm^{-3} of fluorine atoms are contained as impurities in the gate oxide layer of this embodiment, the impurity material is not limited to fluorine, but any of B, C, N, F, P, S, Cl, As, Se, and Br atoms can be used. This can be said for the other embodiments described below. The present inventor has known from experiments that such atoms can be used.

(Second Embodiment)

Next, the second embodiment of the present invention will be described below with reference to Figs. 2(a) − 2(f) and 7. The second embodiment is a method of manufacturing a semiconductor device. Figs. 2(a) − 2(f) show the manufacturing steps thereof.

First, an n-type silicon substrate 1 having, e.g., a surface orientation (100) and a specific resistance of 4 − 6 Ωcm is prepared. Device isolation regions 2a and 2b of about 0.6 μm in depth are formed in the n-type silicon substrate near its surface by a normal shallow trench isolation (STI) method (Fig. 2(a)).

Next, the workpiece is subjected to a mixed gas containing oxygen gas and hydrogen gas at a temperature of, e.g., 750°C in order to form an oxide layer 4 of, e.g., about 3 − 8 nm in thickness. A polycrystalline silicon layer 5 having a thickness of 200 nm, which will serve as a gate electrode, is formed on the oxide layer 4 (Fig. 2(b).

Thereafter, a resist 8 is applied to the entire surface, and then is removed by the resist etch back method, in which the workpiece is soaked in a chemical solution containing 3 kg of hydrogen peroxide solution and 5 kg of sulfuric acid for about 10 minutes. As a result, the resist partially remains on the upper surface of the polycrystalline silicon layer 5, the remaining resist having a height of 100 nm. Subsequently, the dose amount

1×10^{14} cm^{-2} of fluorine ions 6 are injected at an acceleration voltage of, e.g., 10 keV, so that the polycrystalline silicon layer 5 contains fluorine atoms (Fig. 2(c)).

Then, the workpeice is subjected to nitride gas at a temperature of, e.g., 1,000°C for 10 seconds, so that the fluorine atoms in the polycrystalline silicon layer 5 are diffused into the oxide layer 4. Since the fluorine atoms have not been evenly injected to the polycrystalline silicon layer 5, the fluorine concentration distribution in a surface of the gate oxide layer 4 that is parallel to the surface of the silicon substrate 1 is irregular, as indicated by the dotted line (Fig. 2(d)). It is possible that in the step shown in Fig. 2(c), the implantation of fluorine ions can be performed several times, so that the concentration distribution becomes uneven due to the fluctuations during the ion implantation. Since the resist is partially left in the step shown in Fig. 2(c), when ions are implanted to such a coarse surface, the profile of the implanted atoms fluctuates, resulting in that the profile of the atoms implanted into the gate dielectric film through the thermal treatment, which is performed later, also fluctuates. Accordingly, the influence of the atoms on the layer properties becomes irregular.

Fig. 5 shows the change in distribution of Qbd the total amount Qbd of electrons passing through the gate oxide layer before a dielectric breakdown occurs, when the dose amount of fluorine is changed. In Fig. 5, the abscissa axis shows total passing electron amount, Qbd, and the ordinate axis cumulative failure ln(-ln(1-F)). As can be understood from Fig. 5, when the dose amount of fluorine exceeds 1×10^{15} cm^{-2}, the lifetime of devices is abruptly shortened. That is, in a region containing an excessive amount of fluorine atoms, the deterioration of the gate oxide layer is accelerated. It has been verified that the fluorine atom concentration in the gate oxide layer when the dose amount is 1×10^{15} cm^{-2} is more than two times the fluorine atom concentration when the dose amount is 1×10^{14} cm^{-2}. In Fig. 5, Tox means gate oxide layer thickness, and Jg means stress current density.

Fig. 5 will be explained in more detail below.

The present inventor noticed the function of F atoms to improve the reliability of oxide layer, based on the research finding that the distribution in wafer surface of Qbd of p-type polycrystalline silicon (p-Si) gate transistor obtained by implanting ions of boron difluoride (BF_2) is highly uniform.

In order to dope F atoms into the oxide layer, first F ions are implanted to the polycrystalline silicon layer deposited on the gate oxide layer as a gate electrode through the ion implantation method, and then the heat treatment is performed to diffuse the F atoms in the polycrystalline silicon layer into the gate oxide layer. This technique is simple, but is highly compatible with the currently-performed LSI processes. In Fig. 5, the relationship between the Qbd and the cumulative fraction defective $ln(-ln(1-F))$ is plotted (Weibull plots) with respect to an oxide layer in which no F atoms are doped, and oxide layers in which F atoms are doped to certain degrees. As shown in Fig. 5, when F atoms are dopeed into the gate oxide layer, the average Qbd values are not changed (degraded) from those of the oxide layer to which no F atoms are dopeed, but only the lowest (lip) portion in the distribution disappears. On the other hand, when excessive amount of F atoms are dopeed, the entire Qbd values are changed to smaller values. Thus, it can be understood that there is an optimum value for the dopeion amount of F atoms.

This experimental fact suggests that it is important as a technique to improve the reliability of devices that F atoms are dopeed into a gate oxide layer. At the same time, this experimental fact gives an important sign to the analysis of the reason why the electric reliability is improved by dopeing third atoms to a gate oxide layer besides Si atoms and O atoms.

Next, the gate electrode 5a and the gate dielectric film 4a in the MOS transistor region are formed by etching the polycrystalline silicon layer 5 and the oxide layer 4 through reactive ion etching utilizing a resist mask. After the resist mask is removed, diffusion layer regions 10 are formed by implanting the dose amount 5×10^{14} cm^{-2} of BF_2 ions at an acceleration voltage of 30 keV. Subsequently, a sidewall dielectric film 11 of silicon

nitride having a thickness of, e.g., 10 nm, is formed at the sidewall portion of the gate section by the low-pressure chemical vapor deposition (LP-CVD) method (Fig. 2(e)).

Further, a heat treatment is performed on the workpiece
5   in a nitrogen atmosphere at a temperature of e.g., 750 - 950°C for 1 - 100 minutes so as to activate the dopant in the gate electrode and the dopant in the source and drain diffusion layers. Then, a silicon oxide layer 14 having a thickness of, e.g., 300 nm, is deposited on the entire surface through the chemical vapor
10   deposition (CVD) method. Thereafter, contact holes 15 are formed through the silicon oxide layer 14 by anisotropy dry etching. Then, an aluminum layer containing, e.g., 0.5% each of silicon and copper, and having a thickness of 800 nm, is formed and patterned to make aluminum electrodes 16. Finally, the workpiece is heat
15   treated in a nitrogen atmosphere containing 10% hydrogen at a temperature of 450°C for 15 minutes (Fig. 2(f)).

Through the above-described process, a p-channel MOS transistor according to the second embodiment of the present invention is completed.

20   Figs. 6 and 7 show the Weibull plot of the total amount Qbd of electrons in a MOS capacitor utilizing a gate dielectric film according to the embodiment of the present invention, and the initial failure frequency of such MOS capacitors, respectively. In Figs. 6 and 7, Vg means gate voltage, N means sample number
25   and SBD(@initial) means initial soft break down. That is, Fig. 6 shows the Weibull plot of the total amount Qbd of electrons passing through the gate oxide layer before the gate oxide layer reaches a dielectric breakdown state. The device area in this case is 0.1 mm^2. The vertical axis represents values corresponding
30   to the cumulative fraction defective, and the horizontal axis represents Qbd. The black squares represent the experimental results of conventional devices where the impurity atom concentration in the gate dielectric film is not at random, all of these devices first suffering hard breakdown. The black circles
35   represent the measurement results of devices first suffering soft breakdown, obtained by the method of this embodiment, and the

white triangles represent the measurement results of devices first suffering hard breakdown, obtained by the method of this embodiment. As can be clearly understood from Fig. 6, when the method of this embodiment is used, the ratio of devices first suffering the soft breakdown increases. Fig. 7 shows the frequency of occurrence of device first suffering soft breakdown when current-voltage characteristic of a MOS capacitor, having a relatively large area of $1 mm^2$, is measured. With respect to the devices obtained through the process of the present invention (marked "Damaged"), soft breakdown is observed for about 80% of the MOS capacitors. On the other hand, with respect to the devices obtained through the conventional process (marked "Reference"), soft breakdown is observed for only about 5% of the MOS capacitors. Thus, there is a clear difference between the two. It can be understood from Figs. 6 and 7 that soft breakdown is caused very efficiently when the gate oxide layer of the present invention is used for a MOS capacitor.

(Third Embodiment)

Next, the third embodiment of the present invention will be described with reference to Figs. 3(a) to 3(f). The third embodiment is a method of manufacturing a semiconductor device, and Figs. 3(a) to 3(f) show the steps of manufacturing a p-channel MOS transistor of the semiconductor device.

First, an n-type silicon substrate 1 having, e.g., a surface orientation (100) and a specific resistance of $4 - 6 \Omega cm$ is prepared. Device isolation regions 2a and 2b of about 0.6 μm in depth are formed in the n-type silicon substrate 1 near its surface by the normal shallow trench isolation (STI) method (Fig. 3(a)).

Next, the workpiece is subjected to a mixed gas containing oxygen gas and hydrogen gas at a temperature of, e.g., 750°C, in order to form an oxide layer 4 of, e.g., about 3 - 8 nm in thickness. A polycrystalline silicon layer 5 having a thickness of 200 nm, which serves as a gate electrode, is formed on the oxide layer 4 (Fig. 3(b)).

Then, projections and depressions are formed on the upper

surface of the polycrystalline silicon layer 5 through, e.g., chemical dry etching method. In this manner, the effect of the fast etching speed at the grain boundary, and the facet on the (111) surface, which causes fluctuations, can be anticipated. Then, the dose amount 1×10^{14} cm^{-2} of fluorine ions 6 is implanted at an acceleration voltage of 10 keV, thereby implanting fluorine atoms to the polycrystalline silicon layer 5 (Fig. 3(c)). In stead of the above chemical dry etching method, wet etching may be used.

Then, the workpeice is subjected to nitride gas at a temperature of, e.g., 1,000°C for 10 seconds, so that the fluorine atoms in the polycrystalline silicon layer 5 are diffused into the oxide layer 4. Since the fluorine atoms have not been evenly implanted to the polycrystalline silicon layer 5, the fluorine concentration distribution in a surface of the gate oxide layer 4 that is parallel to the surface of the silicon substrate 1 is irregular, as indicated by the dotted line (Fig. 3(d)).

Thereafter, the gate electrode 5a in the MOS transistor region is formed by etching the polycrystalline silicon layer 5 through reactive ion etching utilizing a resist mask. After the resist mask is removed, diffusion layer regions 10 are formed by implanting the dose amount 5×10^{14} cm^{-2} of BF_2 ions 6 at an acceleration voltage of 20 keV. Subsequently, a sidewall dielectric film 11 of silicon nitride having a thickness of, e.g., 10 nm, is formed at the sidewall portion of the gate section by the low-pressure chemical vapor deposition (LP-CVD) method. Then, the dose amount 3×10^{14} cm^{-2} of BF_2 ions 6 are implanted at an acceleration voltage of, e.g., 20 keV to form source and drain diffusion layers 13 (Fig. 3(e)).

Further, a heat treatment is performed on the workpiece in a nitrogen atmosphere at a temperature of e.g., 750 – 950°C for 1 – 100 minutes so as to activate the dopant in the gate electrode and the dopant in the source and drain diffusion layers. Then, a silicon oxide layer 14 having a thickness of, e.g., 300 nm, is deposited on the entire surface trough the chemical vapor deposition (CVD) method. Thereafter, contact holes 15 are formed through the silicon oxide layer 14 by anisotropy dry etching.

Then, an aluminum layer containing, e.g., 0.5% each of silicon and copper, and having a thickness of 800 nm, is formed and patterned to make aluminum electrodes 16. Finally, the workpiece is heat treated in a nitrogen atmosphere containing 10% hydrogen at a
5   temperature of 450°C for 15 minutes (Fig. 3(f)).

In this way, a p-channel MOS transistor according to the third embodiment of the present invention is completed.

(Fourth Embodiment)
10   Figs. 4(a) to 4(f) are sectional views showing the steps of a method of manufacturing a p-channel MOS transistor according to the fourth embodiment of the present invention.

First, an n-type silicon substrate 1 having, e.g., a surface orientation (100) and a specific resistance of 4 − 6 Ωcm is prepared.
15   Device isolation regions 2a and 2b of about 0.6 μm in depth are formed in the n-type silicon substrate 1 near its surface by the normal shallow trench isolation (STI) method (Fig. 4(a)).

Next, the workpiece is subjected to a mixed gas containing oxygen gas and hydrogen gas at a temperature of, e.g., 750°C in
20   order to form an oxide layer 4 of, e.g., about 3 − 8 nm in thickness. A polycrystalline silicon layer 5 having a thickness of 200 nm, which serves as a gate electrode, is formed on the oxide layer 4 (Fig. 4(b)).

Then, a resist is applied to the back surface of the silicon
25   substrate 1. Subsequently, the workpiece is soaked in a 1% potassium hydroxide solution for, e.g., one minute so as to form projections and depressions on the upper surface of the polycrystalline silicon layer 5. After the resist is removed, the dose amount 1 x 10^{14} cm^{-2} of fluorine ions 6 are implanted at
30   an acceleration voltage of 10 kev so as to implant fluorine atoms to the polycrystalline silicon layer 5 (Fig. 4(c)).

Then, the workpeice is subjected to nitride gas at a temperature of, e.g., 1,000°C for 10 seconds, so that the fluorine atoms in the polycrystalline silicon layer 5 are diffused into
35   the oxide layer 4. Since the fluorine atoms have not been evenly implanted to the polycrystalline silicon layer 5, the fluorine

concentration distribution in a surface of the gate oxide layer 4 that is parallel to the surface of the silicon substrate 1 is irregular, as shown by the dotted line (Fig. 4(d)).

Thereafter, the gate electrode 5a and the gate oxide layer 4a in the MOS transistor region are formed by etching the polycrystalline silicon layer 5 and the oxide layer 4 through reactive ion etching utilizing a resist mask. After the resist mask is removed, diffusion layer regions 10 are formed by implanting the dose amount 5×10^{14} cm^{-2} of BF_2 ions 6 at an acceleration voltage of 20 keV. Subsequently, a sidewall dielectric film 11 of silicon nitride having a thickness of, e.g., 10 nm is formed at the sidewall portion of the gate section by the low-pressure chemical vapor deposition (LP-CVD) method (Fig. 4(e)).

Further, a heat treatment is performed on the workpiece in a nitrogen atmosphere at a temperature of e.g., 750 - 950°C for 1 - 100 minutes so as to activate the dopant in the gate electrode and the dopant in the source and drain diffusion layers. Then, a silicon oxide layer 14 having a thickness of, e.g., 300 nm, is deposited on the entire surface through the chemical vapor deposition (CVD) method. Thereafter, contact holes 15 are formed through the silicon oxide layer 14 by anisotropy dry etching. Then, an aluminum layer containing, e.g., 0.5% each of silicon and copper, and having a thickness of 800 nm, is formed and patterned to make aluminum electrodes 16. Finally, the workpiece is heat treated in a nitrogen atmosphere containing 10% hydrogen at a temperature of 450°C for 15 minutes (Fig. 4(f)).

In this way, a p-channel MOS transistor according to the fourth embodiment of the present invention is completed.

Although a thermally-oxidized silicon layer is used as the gate dielectric film of the embodiments of the present invention, the material is not limited thereto. It is possible to use an oxide layer containing nitrogen, a nitride layer, or any other high-k material layer. Further, an oxide layer using oxygen activated by the use of microwaves or laser has the same effects as a thermally-oxidized layer. Moreover, the present invention can be applied to a device using the fluctuations caused by the

breakdown phenomenon. The present invention can be modified further as long as the modification does not veer from the scope of the present invention.

As described above, according to the present invention,
5   it is possible to prevent the dielectric breakdown of a gate dielectric film from proceeding from soft breakdown, thereby elongating the hard breakdown lifetime of the gate dielectric film. It is also possible to form a MOS transistor including such a gate dielectric film and having a high reliability with a
10   relatively easy method.

Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details and
15   representative embodiments shown and described herein. Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concepts as defined by the appended claims and their equivalents.